[Total No. of Questions - 9] [Total No. of ted Pages - 2] (2126)

16192(D) OEC 2016

B. Tech 7th Semester Examination Digital System Design Using HDL (NS) EC-412

Time: 3 Hours Max. Marks: 100

The candidates shall limit their answers precisely within the answerbook (40 pages) issued to them and no supplementary/continuation sheet will be issued.

- **Note:** (i) Attempt five questions in all selecting one question each from sections A, B, C & D. Section-E is compulsory.
 - (ii) All parts of a question should be answered at one place.
 - (iii) Answers should be brief and to-the-point supplemented with neat sketches.

SECTION - A

- (a) Define the different behavioral and structural models. Write the code for a half subtractor using behavioral models. (10)
 - (b) Explain the different types of operators and data types. (10)
- 2. (a) What are assignment statements and two dimensional arrays? Enlist a process to read from the array, (10)
 - (b) Define functions and explain the significance of function applications. (10)

SECTION - B

- (a) Design a MOD-10 counter using T flip-flop with its coding processes. (10)
 - (b) Design a 4- bit shift register and enlist the test bench for verification. (10)
- 4. (a) What are multiplexers? Design a 16:1 multiplexer tree using 8:1 data selectors. (10)

(b) What is the significance of BCD code? Design a 4-bit decimal to BCD code converter circuit. (10)

SECTION - C

- 5. (a) Describe the significance of DMA. Implement a DMA and control register. (10)
 - (b) Implement a microprocessor register block for checking the configuration as well as the status. (10)
- (a) Define DRAM. Describe the different structures of DRAM.
 (10)
 - (b) Explain the significance of skewed clock with its merits and demerits. (10)

SECTION - D

- 7. (a) Describe the PAL and its applications. Design a function $f=\Sigma(0,3,4,5,6)$ using PAL. (10)
 - (b) Explain the FIR filter design using the flow charts. (10)
- 8. (a) Explain the different classes of verifications with suitable examples. (10)
 - (b) What are the ASIC design procedures? Explain the design partition process. (10)

SECTION - E

- 9. (a) Enlist the delays and their significance in digital design.
 - (b) Elaborate the process of code customization using generics.
 - (c) What is universal shift register?
 - (d) Enlist the applications of flip-flops.
 - (e) What is carry ripple adder circuit?
 - (f) Describe the register block synthesis process.
 - (g) What is the difference between gated clock and skew clock?
 - (h) Define FIFO.

(2½×8=20)